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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,255	09/12/2000	Russell Byrd	42390.P8718	6781

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Charles K Young
Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026

EXAMINER	
PHAM, TUAN	

ART UNIT	PAPER NUMBER
2643	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/660,255	Applicant(s) BYRD ET AL.	
	Examiner TUAN A PHAM	Art Unit 2643	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Frantz et al. (U.S. Patent No. 5,802,169, hereinafter, "Frantz").

Regarding claim 11, Frantz teaches an integrated circuit comprising:

a receiver to receive a signal from a transport medium, the receiver having a ring input and a tip input (see figure 1, col.3, ln.46-67); and

a programmable resistor to provide a resistance between the ring input and the tip input, the resistance being electronically programmable (see figure 1, adjustable impedance 112, col.3, ln.46-67).

Regarding claim 12, Frantz further teaches the integrated circuit further comprising: a register coupled to the programmable resistor, wherein the resistance is electronically programmed by writing to the register (see col.6, ln.5-20).

3. Claims 15-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Armistead et al. (U.S. Patent No. 6,553,117, hereinafter, "Armistead").

Regarding claim 15, Armistead teaches a method of tuning a resistance of an integrated circuit (IC) comprising:

determining the resistance of the IC corresponding to a first configuration of parallel resistors, wherein a portion of the parallel resistors are enabled (see figure 7, R1-R5, col.6, ln.1-15, col.7, ln.5-14); and

modifying the resistance of the IC by creating a second configuration of parallel resistors, wherein a different portion of the parallel resistors are enabled (see col.7, ln.5-14).

Regarding claim 16, Armistead further teaches the method modifying the resistance is performed by writing to a register (i.e. programmable logic) on the IC (see col.6, ln.1-17).

Regarding claim 17, Armistead further teaches the method further comprising: permanently disabling a subsequent modification of the second configuration of

parallel resistors (see col.4, ln.50-60).

Regarding claim 18, Armistead further teaches the method further comprising: controlling the entire second configuration of parallel resistors to be enabled and disabled (see col.4, ln.50-60).

Regarding claim 19, Armistead further teaches the method permanently disabling of a subsequent modification is achieved by blowing a fuse on the IC (see col.4, ln.50-60).

Regarding claim 20, Armistead further teaches the method modifying the resistance of the IC is performed by enabling a resistor of the parallel resistors to reduce the resistance of the IC by a predetermined percentage (see col.7, ln.5-14).

Regarding claim 21, Armistead further teaches the method modifying the resistance of the IC is performed by disabling a resistor of the parallel resistors to increase the resistance of the IC by a predetermined percentage (see col.4, ln.45-65).

Regarding claim 22, Armistead teaches a line interface having a programmable resistor, a method of matching an impedance of a transport medium (see figure 7, impedance matching circuit 68) comprising:

writing to a register (i.e. programmable logic) that controls the programmable resistor (see col.4, ln.45-65); and

changing the programmable resistor to provide effective impedance substantially matching the impedance of the transport medium responsive to writing to the register (see col.6, ln.1-17).

Regarding claim 23, Armistead further teaches the method changing the programmable resistor is accomplished by disabling the programmable resistor (see col.4, ln.45-65).

Regarding claim 24, Armistead further teaches the method further comprising: coupling the line interface to the transport medium (see col.4, ln.45-65).

Regarding claim 25, Armistead further teaches the method the transport medium supports a T1, J1, or E1 transport protocol (see col.4, ln.45-65).

Regarding claim 26, Armistead further teaches the method the programmable resistor is changed to provide the effective impedance of 75 ohms, 100 ohms, 110 ohms, or 120 ohms (see col.6, ln.20-30).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Frantz et al. (U.S. Patent No. 5,802,169, hereinafter, "Frantz").

Regarding claim 1, the prior art teaches a line interface for coupling to a first transport medium (see figure 1), the line interface comprising:

an external resistor coupled in parallel with the transceiver to provide a first effective impedance to substantially match an impedance of the first transport medium (see figure 1, resistor 130, transceiver 150).

It should be noticed that the prior art fails to teach an integrated circuit comprising a programmable resistor (i.e. adjustable hybrid circuit). However, Frantz teaches such features (see figure 1, adjustable hybrid circuit 111, col.3, ln.55-63) for a purpose of automatically determining the impedance of a subscriber line interface.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of an integrated circuit comprising a programmable resistor, as taught by Frantz, into view of prior art in order to improve the maximum the power transfer of a subscriber line interface.

7. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frantz et al. (U.S. Patent No. 5,802,169, hereinafter, "Frantz") in view of Armistead et al. (U.S. Patent No. 6,553,117, hereinafter, "Armistead").

Regarding claim 13, Frantz further teaches an integrated circuit comprising:

a receiver to receive a signal from a transport medium, the receiver having a ring input and a tip input (see figure 1, col.3, ln.46-67);

a programmable resistor to provide a resistance between the ring input and the tip input, the resistance being electronically programmable (see figure 1, adjustable impedance 112, col.3, ln.46-67); and

a register coupled to the programmable resistor, wherein the resistance is electronically programmed by writing to the register (see col.6, ln.5-20).

It should be noticed that Frantz fails to clearly teach the programmable resistor is comprised of a plurality of parallel resistors, and wherein a portion of the plurality of parallel resistors is enabled via a value written to the register. However, Armistead teaches such features (see figure 7, R1-R5, col.6, ln.1-17) for a purpose of automatically determining the impedance of a subscriber line interface.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of programmable resistor is comprised of a plurality of parallel resistors, and wherein a portion of the plurality of parallel resistors is enabled via a value written to the register, as taught by Armistead, into view of Frantz in order to improve the maximum the power transfer of a subscriber line interface.

Regarding claim 14, Armistead further teaches the integrated circuit wherein the programmable resistor is comprised of a plurality of resistors and transmission gates coupled to the plurality of resistors, and wherein the transmission gates are controlled

by writing to the register (i.e. programmable logic) (see figure 7, R1-R5, programmable logic 34, col.6, ln.1-17).

8. Claims 2-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Frantz et al. (U.S. Patent No. 5,802,169, hereinafter, "Frantz") as applied to claim 1 above, and further in view of Armistead et al. (U.S. Patent No. 6,553,117, hereinafter, "Armistead").

Regarding claim 2, prior art and Frantz, in combination, fails to clearly teach the programmable resistor and the external resistor are coupled to provide a second effective impedance to substantially match an impedance of a second transport medium, wherein the impedance of the first transport medium is different from the impedance of the second transport medium. However, Armistead teaches such features (see col.6, ln.1-17) for a purpose of automatically determining the impedance of a subscriber line interface.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of the programmable resistor and the external resistor are coupled to provide a second effective impedance to substantially match an impedance of a second transport medium, wherein the impedance of the first transport medium is different from the impedance of the second transport medium, as taught by Armistead, into view of prior art and Frantz in order to improve the maximum the power transfer of a subscriber line interface.

Regarding claim 3, Armistead further teaches the line interface wherein the impedance of the second transport medium substantially matches 75 ohms, 100 ohms or 110 ohms (see col.6, ln.20-29).

Regarding claim 4, Armistead further teaches the line interface wherein the first transport medium is a TI line and the second transport medium is a J1 line (see col.4, ln.45-65).

Regarding claim 5, Armistead further teaches the line interface wherein the first transport medium is a T1 line and the second transport medium is an E1 line (see col.4, ln.55-60).

Regarding claim 6, Frantz further teaches the line interface wherein the programmable resistor and external resistor are coupled to provide a second impedance to substantially match an impedance of a second transport medium responsive to a write to a register of the integrated circuit (see col.6, ln.5-20).

Regarding claim 7, Armistead further teaches the line interface wherein the impedance of the first transport medium substantially matches 75 ohms, 100 ohms or 110 ohms (see col.6, ln.20-29).

Regarding claim 8, Armistead further teaches the line interface wherein the programmable resistor can be disabled, and wherein the external resistor substantially matches 120 ohms (see col.6, ln.20-29).

Regarding claim 9, Armistead further teaches the line interface wherein the integrated circuit comprises a second programmable resistor to couple to a secondary transport medium (see col.6, ln.1-15).

Regarding claim 10, Armistead further teaches the line interface wherein the first transport medium has a first impedance and the secondary transport medium has a second impedance, and wherein the first impedance is different from the second impedance (see col.4, ln.50-60).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In order to expedite the prosecution of this application, the applicants are also requested to consider the following references. Although Dahan et al. (U.S. Patent No. 6,611,580), Gorcea et al. (U.S. Patent No. 6,665,399), Madonna et al. (U.S. Patent No. 5,596,569), and Kwon (U.S. Patent No. 6,330,138) are not applied into this Office Action, they are also called to Applicants attention. They may be used in future Office Action(s). These references are also concerned for supporting the system and method for adaptively adjusting modem operating characteristics and impedance matching circuit.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tuan A. Pham** whose telephone number is (703) 305-4987 and E-mail address is: **tuan.pham@USPTO.GOV**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Curtis Kuntz, can be reached on (703) 305-4708 and

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Art Unit 2643

Date: February 26, 2004

Examiner

Tuan Pham

BINH TIEU
PRIMARY EXAMINER